Application No.: 09/751,761

Response to Final Office Action dated: September 26, 2006

Final Office Action dated: June 26, 2006

RECEIVED CENTRAL FAX CENTER

SEP 2 6 2006

## REMARKS/ARGUMENTS

Claims 20-38 are pending in the application. Claims 1-19 have been previously cancelled. Applicant thanks the Examiner for acknowledging the receipt of the Extension of Time and Amendment filed.

## Claim Objections

Claim 28 is objected to due to informalities. Applicant has made appropriate corrections and requests that the objections be withdrawn.

## Claim Rejections Under 35 U.S.C. §103(a)

Claims 20, 24, 26, 33, and 37 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,643,803 (hereinafter referred to as Swoboda) in view U.S. Patent No. 5,551,050 (hereinafter referred to as Ehlig). Claims 21, 27, and 34 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Swoboda in view of Ehlig and further in view of U.S. Patent No. 5,903,768 (hereinafter Sato). Claims 22-23, 25, 28-30, 35-36, and 38 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Swoboda in view of Ehlig and further in view of U.S. Patent No. 6,285,974 (hereinafter referred to as Mandyam). Claims 31-32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Swoboda in view of Ehlig in view of Mandyam and further in view of Hennessy and Patterson, Computer Organization and Design, 2<sup>nd</sup> Edition, 1998 (hereinafter referred to as Hennessy).

Page 3 section 6e of the Office Action dated June 26, 2006 admits that Swoboda does not teach comparing the architectural state value for the processor core to an architectural state value for a second processor core. The Office Action claims this deficiency is made up for in Ehlig,

Application No.: 09/751,761

Response to Final Office Action dated: September 26, 2006

Final Office Action dated: June 26, 2006

which according to the Office Action, teaches "the concept of comparing first processor data obtained from emulation circuitry to second processor data obtained from emulation circuitry." Ehlig, however, does not teach applicant's claimed invention because the processor data in Ehlig is different than an architectural state value of a processor core.

Additionally, applicant asserts that neither Swoboda nor Ehlig teach "executing said neutral instruction to ascertain an architectural state value for said processor core." On page 3 at section 6d, the Office Action asserts that claim 1 and the abstract of Swoboda teach this element, but applicant cannot find anywhere in the Swoboda reference where ascertaining an architectural state value from a neutral instruction is taught. The office action states that the cited sections of Swoboda teach receiving a value, but it appears Swoboda is referring to receiving instructions, not architectural state values of processor cores. It is also not apparent in Swoboda that whatever value the office action is referring to is being received as the result of executing a neutral instruction.

In light of the preceding discussion, it is also apparent that no motivation to combine the Swoboda reference and the Ehlig reference exists. Swoboda teaches a processor that can enter a debug suspend state in response to a debug event and then leave the debug suspend state in order to resume normal operation. See Swoboda at column 2, lines 53-60. Swoboda targets the process of debug where debug is defined as being able to detect the effects of and alter the results of the execution of software on the processor. See Abstract. Ehlig teaches synchronizing redundant processors so that data output to memory for the multiple processors can be compared. Because Ehlig is using output data to make its comparisons, there is no need for a neutral instruction. Because Swoboda teaches debug circuitry, there is no need for multiple processors

Application No.: 09/751,761

Response to Final Office Action dated: September 26, 2006

Final Office Action dated: June 26, 2006

and comparisons. The purpose of the debug circuitry is to "fix" the problem, not to determine if an error has occurred by comparing it to a redundant processor. Therefore, there exists no motivation to combine the teachings of Swoboda and Ehlig.

For at least all of the reasons discussed above, applicants assert that independent claims 20, 26, and 33 are in condition for allowance. Applicant also assert that dependent claims 21-25, 27-32, and 34-38 are allowable as depending from allowable independent claims. Therefore, applicants respectfully request that the rejections under 35 U.S.C. § 103(a) be withdrawn.

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. 11-0600.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

Respectfully submitted,

KENYON & KENYON LLP

Dated: September 26, 2006

Jeffrey R. Joseph (Reg. No.54,204)

Attorneys for Intel Corporation

KENYON & KENYON LLP 333 West San Carlos St., Suite 600 San Jose, CA 95110

Telephone:

(408) 975-7500

Facsimile:

(408) 975-7501

SJ01 92710 v1